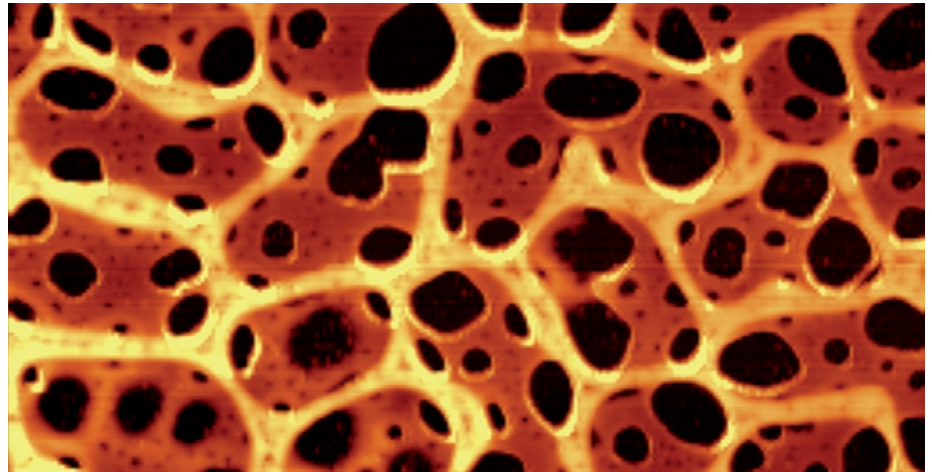


Scanning Probe Microscope Control

New Electronic Concept for Utmost SPM Demands

Controlling the latest Scanning Probe Microscopes (SPMs) demand highly sophisticated electronics. This is apparent when considering even relatively simple operational procedures such as the tip approach of an Atomic Force Microscope (AFM): The controller must lower the tip towards the sample surface while at the same time it must ensure that the tip does not crash into the sample.



This, however, includes several tasks: Generating the signals for a motor to lower the tip, acquiring the return signals from the tip or a 4-Quadrant diode, filtering the acquired signals, computing of the appropriate control signals, outputting them and finally interacting with the user who may want to be updated.

With only one central data processing unit (CPU or DSP), today's SPM controllers can only virtually perform all these tasks in parallel, in reality they have to switch between the different tasks at short intervals. This results in an uneven movement with an indeterministic timing-behavior as any additional task must compete for

processing time, which – as a consequence – affects all other processes.

To overcome these drawbacks and to achieve the best possible results with extremely low noise levels, we have introduced a completely new approach to controlling SPMs with the WITec *alphaControl* (fig. 1).

It uses a Field Programmable Gate Array (FPGA) to implement the SPM controller and all digital controlling tasks, providing unrivalled data processing speed by computing all SPM control tasks in parallel within a single chip.

Field Programmable Gate Arrays Basics

Field Programmable Gate Arrays are semiconductor devices containing programmable logic components, memory elements and programmable interconnects. The programmable logic components can be programmed to duplicate the functionality of basic logic gates such as AND, OR, XOR, NOT or more complex combinatorial functions such as decoders or simple math functions. By using the programmable interconnects, it is possible to connect these basic building blocks to create more sophisticated designs such as microcontrollers, Lock-In amplifiers or, as in the case of the *alphaControl*, extremely powerful SPM controllers. The achieved complexity and

data processing power is limited only by the size of the FPGA. Current FPGAs contain up to tens of thousands of the basic building blocks, with this number increasing rapidly according to Moore's law.

The advantages of an FPGA-based SPM controller over a CPU/DSP-based design become apparent when studying a simple task: the subtraction of two analog signals.

A CPU/DSP with only one processing unit, address and data bus to access its ADCs and DACs has to perform several steps to complete the task:

- 1.) Write Address for ADC1 on Address Bus
- 2.) Read Data from ADC1 in CPU/DSP
- 3.) Write Address for ADC2 on Address Bus
- 4.) Read Data from ADC2 in CPU/DSP
- 5.) Subtract (ADC1 – ADC2) in CPU
- 6.) Write Address for DAC on Address Bus
- 7.) Write Result to Data Bus for DAC (fig. 2)

Each step of the task needs to be performed sequentially one after another. At the same time, other additional tasks compete for CPU time. This results in a complex and often almost indeterministic timing behavior, which makes simultaneous control of different tasks extremely difficult.



Fig. 1: The WITec *alphaControl* controller

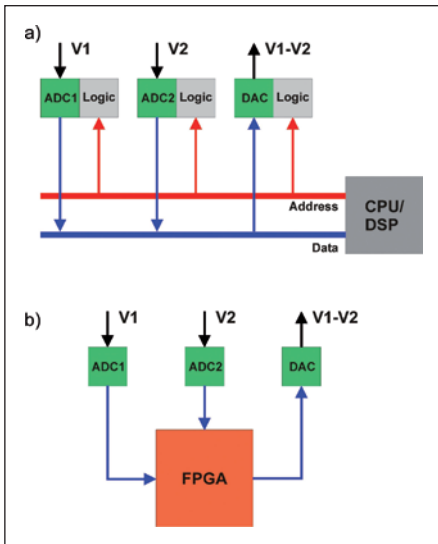


Fig. 2: CPU/DSP based solution (a), Programmed logic solution (b)

In contrast, the FPGA-design, which is based on programmed logic, allows the task to be solved differently by programming the FPGA in such a way that a part of the FPGA resources form a dedicated hardware component for the process. This uses up a small fraction of the FPGA resources, but it allows the problem to be solved in hardware, which is much faster than a step by step execution using a software solution.

Additionally, the ample I/O-resources of the FPGA allow the ADCs and the DAC to be connected permanently with the FPGA in a star-topology.

As many processing units can operate in parallel within the FPGA logic matrix, the entire task can be performed within one clock cycle without being disturbed by other tasks. Performance decreases caused by bus-bottlenecks or task-switching are thus avoided. Calculations are completely independent of and undisturbed by other tasks.

The Controller

To make full use of the advantages of the FPGA architecture, the main controller functionality of the *alphaControl* SPM controller is implemented in the form of a “system-on-a-chip” within one single powerful and in-system re-programmable FPGA. This allows true parallel execution of all controlling tasks with response times of down to a few nanoseconds. At the same time, the full 32 bit digital design guarantees the best possible noise and drift performance (fig. 3).

The FPGA used by the *alphaControl* features two million logic gates running at a clock-rate of 80 MHz. Along with all the standard SPM modes, additional fea-

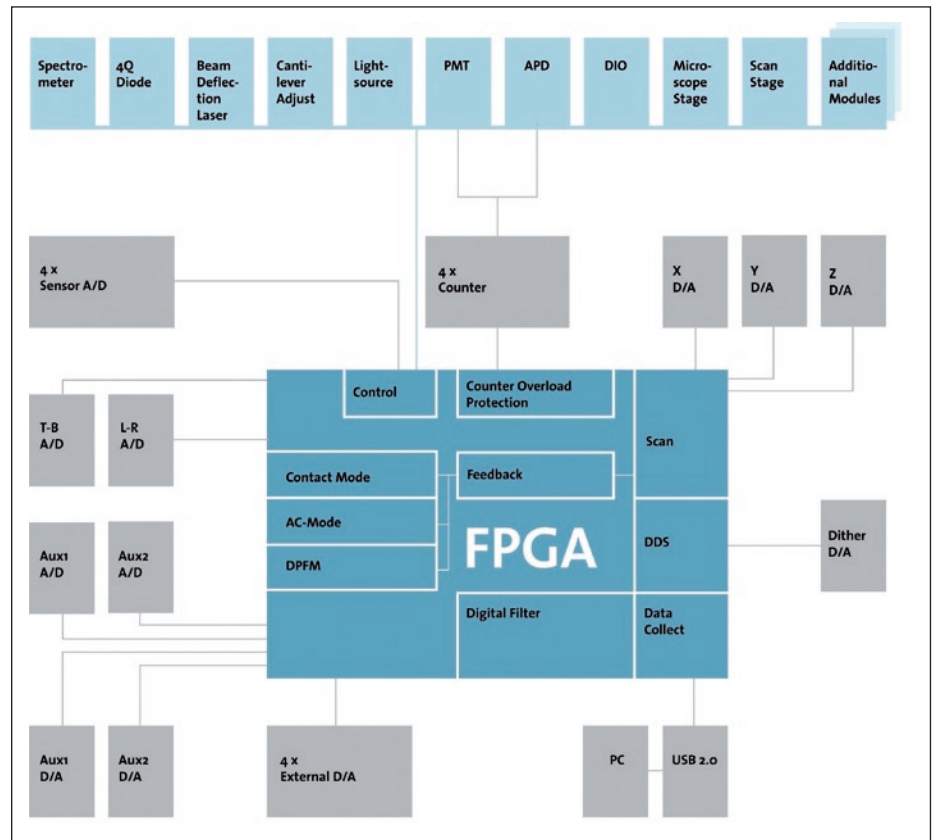


Fig. 3: System on a programmable chip – the star topology

tures including digital filters, Lock-In amplifiers and several high-speed counters (e.g. for single photon sensitive detectors) are implemented within the FPGA matrix, while yet still leaving enough room for future expansion.

Interfacing of the controller with the SPM head is realized by several modular and easily exchangeable A/D or D/A converter boards. The boards are connected to the FPGA in a star topology, making use of the more than 600 I/O pins of the FPGA. As the programming of the FPGA determines which of the I/Os are used for inputs or outputs, an easy upgrade path for higher performance ADCs, DACs, or other extension boards exists.

At the same time, the massive parallel processing power of the FPGA, in conjunction with the star topology, allows the use of extremely fast and precise A/D and D/A converters.

The standard *alphaControl* controller, for example, is equipped with up to four high-speed 16 Bit A/D converters, each running at five MSamples/s to process the signals from the 4-Quadrant photodiode. Such high sampling rates allow detailed studies of tip – sample interaction or can also be used for seamless, all digital, Lock-In implementations, as is necessary for real phase AC-Mode or effective digital filtering for the lowest possible noise levels.

Four additional slower ADCs, with a 200 kHz sampling rate each, are present to read in the sensor values from the capacitive sensors of the scan stage. Three dedicated high resolution DACs, running at 1.25 MHz, are responsible for scanning and enable scan speeds of up to several hundred lines per second. Further DACs available for signal access complete the controllers A/D and D/A capabilities.

The communication of the controller with the host PC is based on an USB2.0 interface. This high speed interface is capable of continuous data transfer rates in the order of several tens of MByte/s.

As this interface is also used to configure the FPGA after starting up the system, the functionality of the *alphaControl* can easily be altered or updated by the standard control software.

The modular design of the *alphaControl* SPM controller is also reflected in its external design: The controller is formed by two racks, the main rack and an extension rack, both located in a convenient and easily accessible housing. The main rack contains the FPGA, the USB interface, all the A/D, D/A converters and counter modules, while the extension rack is reserved for power supplies, motor control units, high voltage amplifiers and laser modules.

In addition to the unique combination of measurement modes, including Atomic

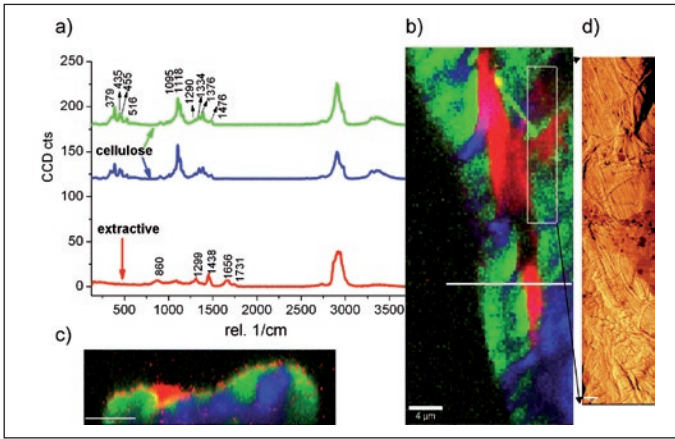


Fig. 4: One instrument, many techniques: these examples show the combination of confocal Raman imaging and atomic force microscopy to study wood extractives on cellulose surfaces. Raman spectra (a), Raman lateral image (b), Raman depth scan (c), AFM phase image (d)

Force Microscopy (AFM), Scanning Near-field Optical Microscopy (SNOM), Confocal Microscopy, Fluorescence Microscopy, and Raman Imaging in a single instrument, the substantial resources of the

FPGA additionally allow implementation of some major improvements over other controller designs (fig. 4).

The control logic of the scans, for example, is designed to handle scans of complete images without interacting with the host PC, instead of line by line scanning. In addition to improving system stability, this leads to true real time control of the scan movement. Short interruptions of the scan movement, e.g. at the end of each scan line, to obtain new data from the host PC, are not necessary. The resulting smooth and deterministic scan movement simplifies the synchronisation with external experiments and reduces bleaching in optical experiments or other scan-induced artefacts.

Another key feature introduced with the *alphaControl* is the *TrueScan* functionality. While standard closed-loop scanners can only account for static positioning errors of the probe, the *TrueScan* technique allows minimization of dynamic positioning errors for the first time. This is achieved by reading the actual scan-stage position and using this information to correct the acquired SPM probe data (fig. 5).

Sample scanning systems in particular, such as SNOMs, can benefit from this improvement. Due to the inertial behavior of the scan stage, a phase shift between the scan stage control voltages and the actual movement of the stage would be observed at high scan rates without *TrueScan*.

The key to using the unique features of the *alphaControl* is the integrated software for measurement control. With its structure, it helps the user navigate through the measurement tasks while intuitively providing a user interface that changes automatically to correspond with the method used. This also reflects the modular concept of the *alpha300* SPM series, which allows the combination of different microscopy techniques – as mentioned above – in a single instrument.

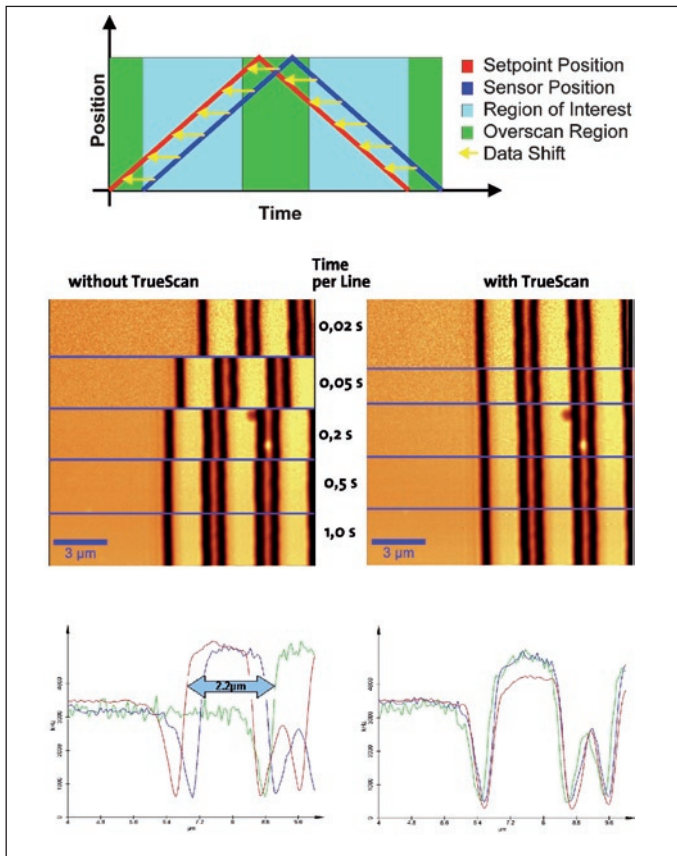


Fig. 5: TrueScan: dynamic position correction. Allows correction of dynamic positioning errors, which is particularly important for fast scans.

Conclusion

We demonstrate a completely new SPM controller design based on an FPGA instead of the conventional DSP/CPU approach.

The time-consuming task of switching between data acquisition, digital filtering, scanning and the computing of feedback signals is eliminated. Together with a star topology to avoid any bus limitations in accessing the variety of ADCs and DACs, this design guarantees an entirely deterministic timing capability in the nano-second regime for all tasks for the first time. This is particularly useful for any external experiment which must be synchronised with the scan, or for high-speed scans, in which in addition to closed-loop control of the scanner, dynamic corrections of the scan movement are necessary.

Delicate samples benefit additionally from extremely high sampling rates, allowing highly resolved signals and low noise levels.

The controller's revolutionary system-on-a-chip concept enhances not only user friendliness but also speed, flexibility, accuracy, expandability and timing precision. It enables a variety of new features and automated measurement procedures to be employed for the first time. The digital signal processing reduces noise to extremely low levels and significantly enhances data and image quality.

The latest generation of microscopes is therefore ideally suited for applications in Materials Sciences, Life Sciences, Pharmaceuticals and Nanotechnology, in which a comprehensive understanding of the sample structure and composition is a necessity.

Contact:

Dr. Peter Spizig
 WITec Wissenschaftliche Instrumente
 und Technologie GmbH, Ulm, Germany
 Tel.: +49 700 94832366
 Fax: +49 700 94832329
 Peter.Spizig@WITec.de
 www.WITec.de